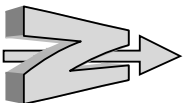


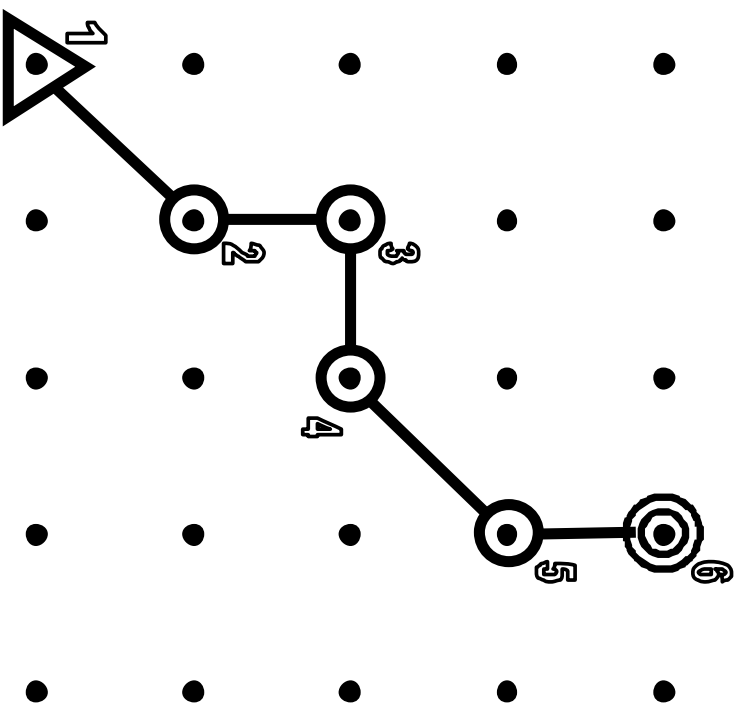
Nom :

Circuit 1

A

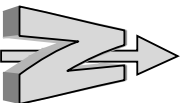


Δ
Départ

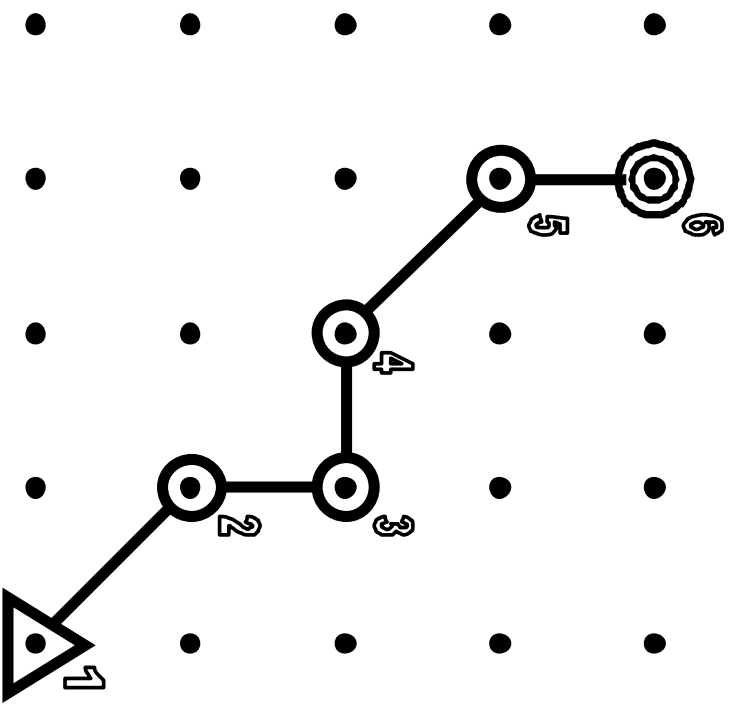
[illegible]

Nom :

Circuit
1
B



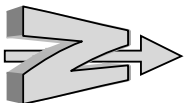
Δ
Départ

[illegible]

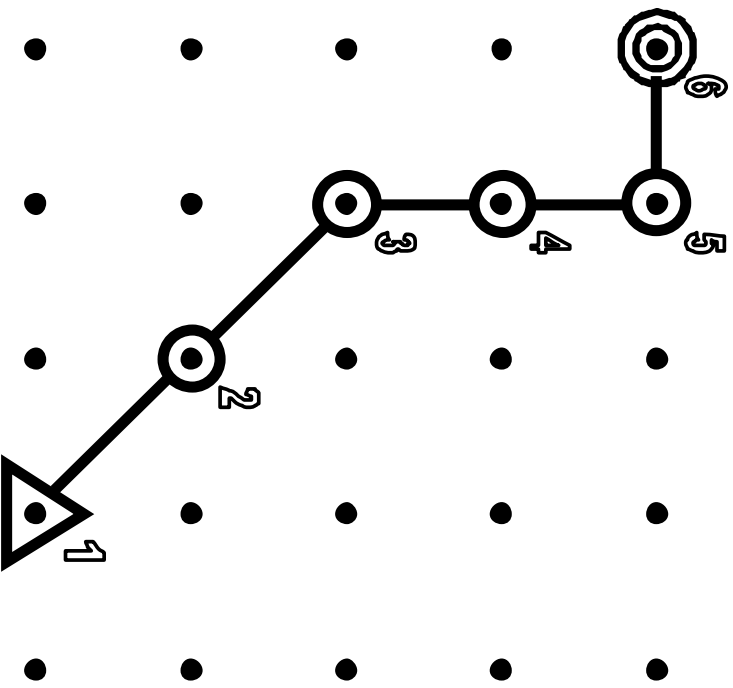
Nom :

Circuit
3
A

ω



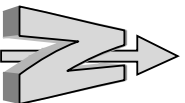
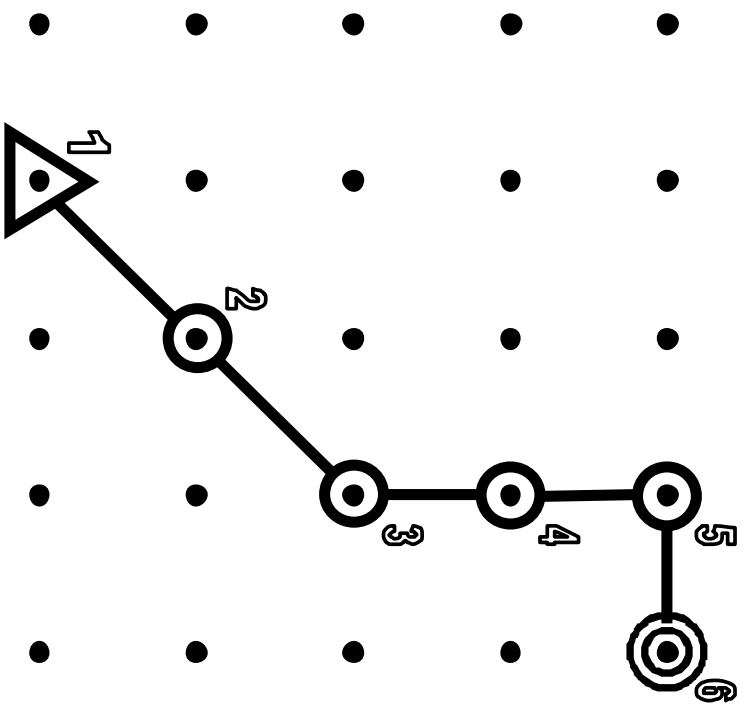
Départ Δ

[illegible]

Nom :

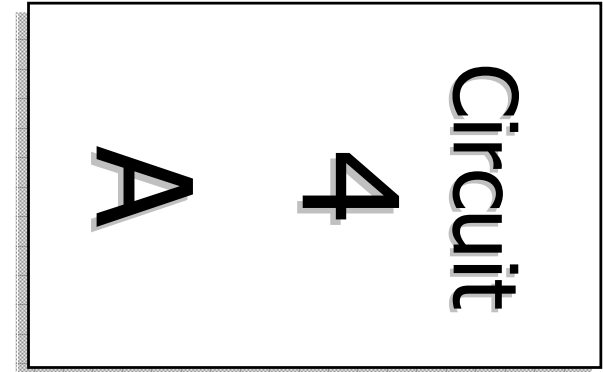
Circuit
3
B

ω

Départ [illegible]

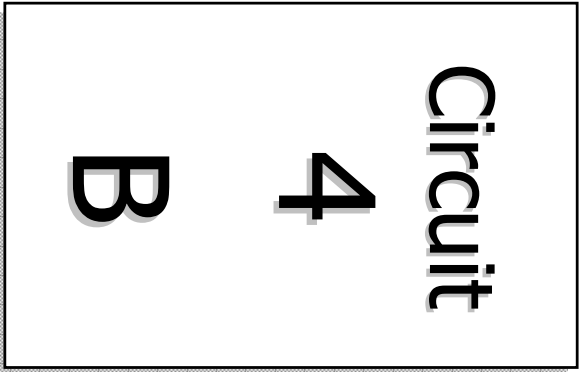
Nom :

4



Nom :

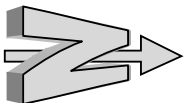
4

[illegible]

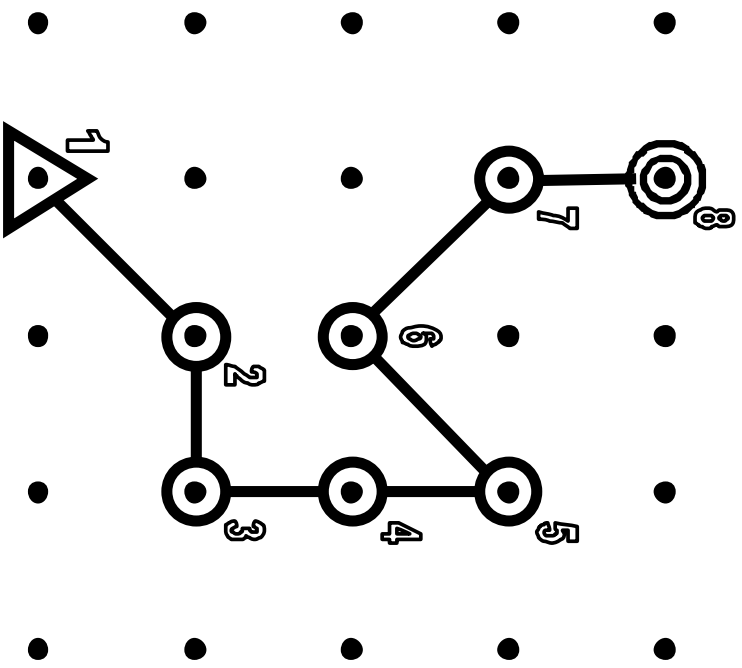
Nom :

Circuit
5
A

ט



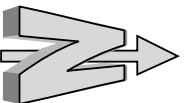
Δ
Départ

[illegible]

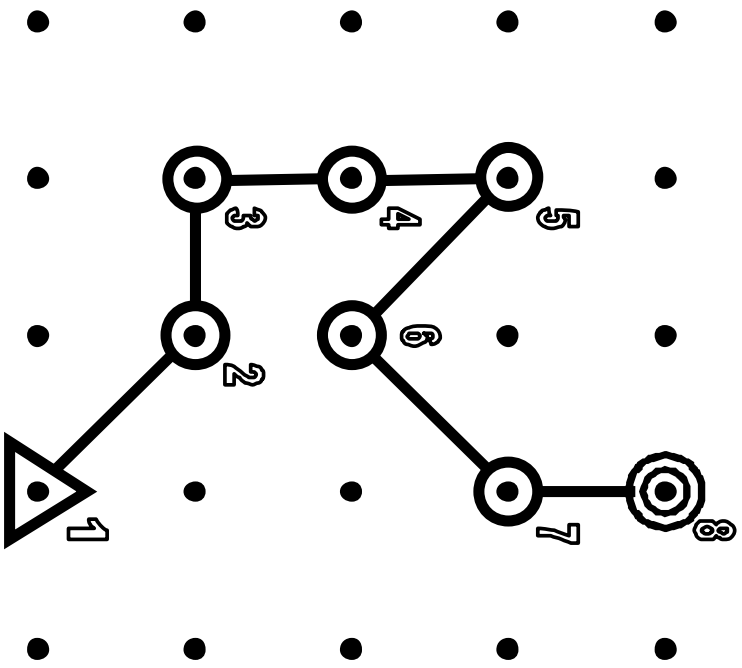
Nom :

Circuit
5
B

ט

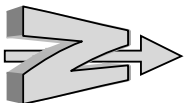


Δ
Départ

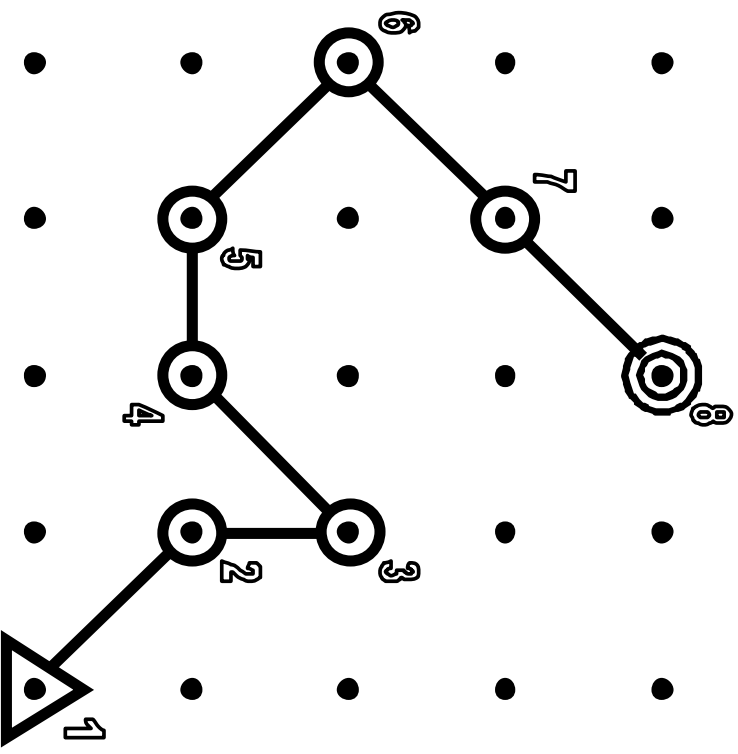
[illegible]

Nom :

Circuit
6
A

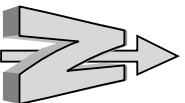


Δ
Départ

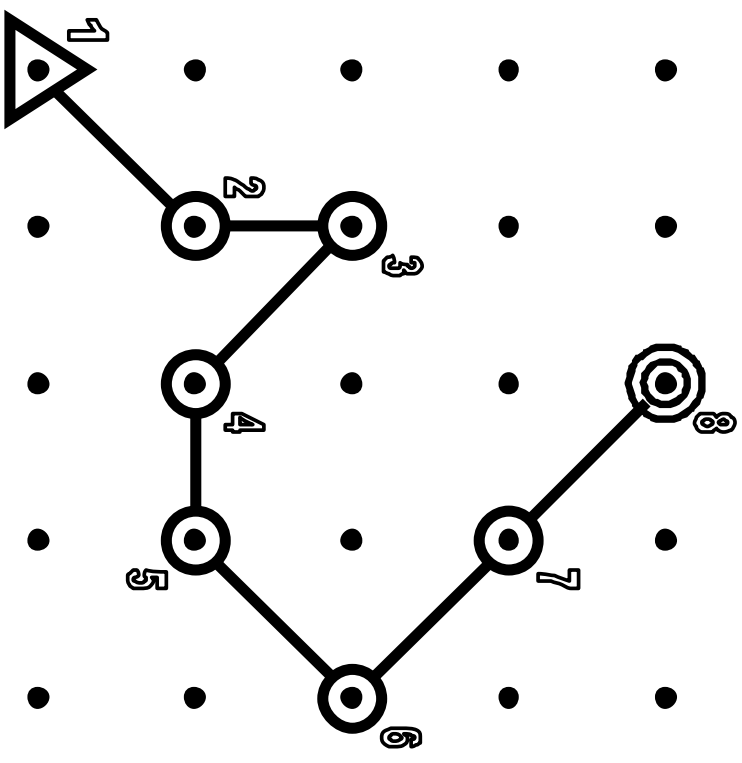
[illegible]

Nom :

Circuit
6
B

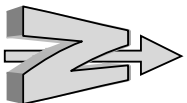


Δ
Départ

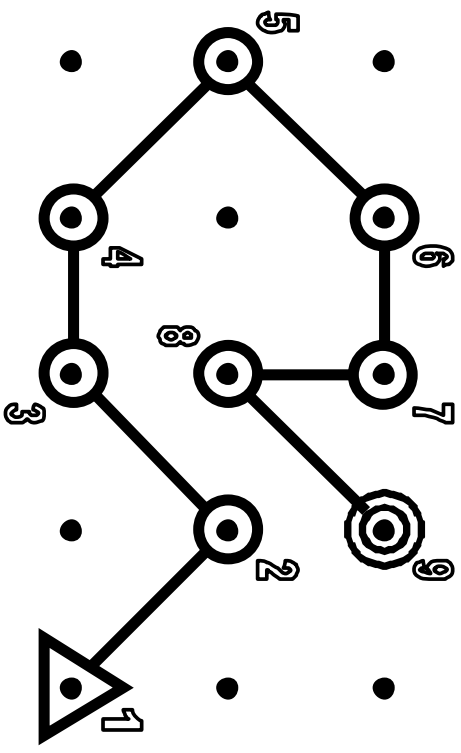
[illegible]

Nom :

Circuit
7
A

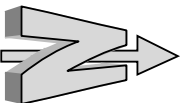
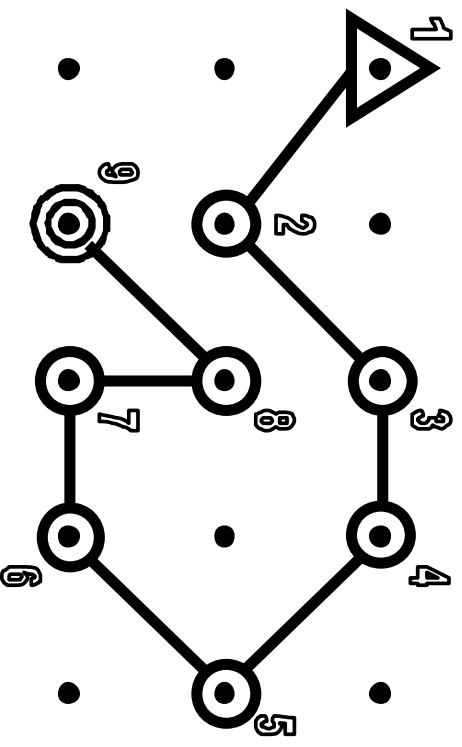


Départ Δ

[illegible]

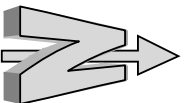
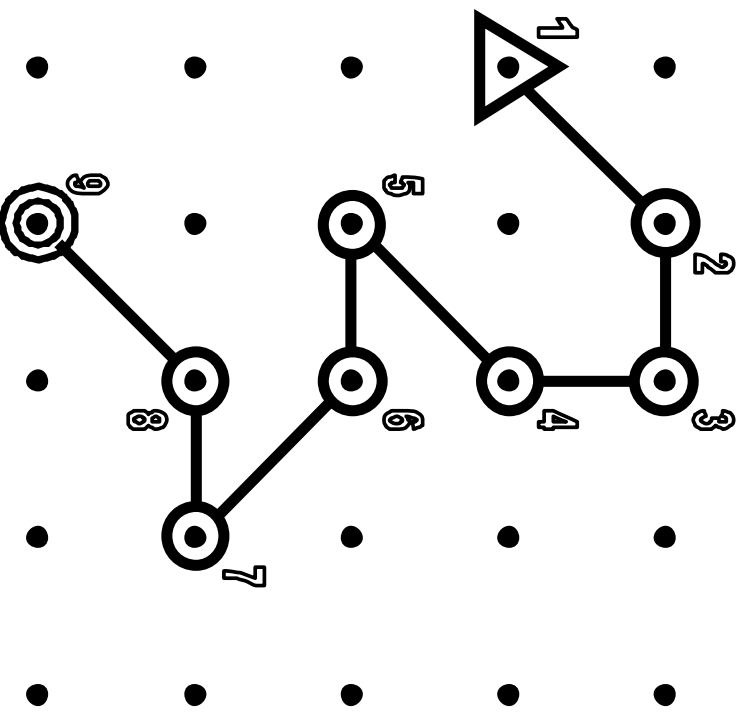
Nom :

Circuit
7
B

Départ [illegible]

Nom :

Circuit
8
A

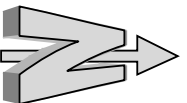
Départ [illegible]

Nom :

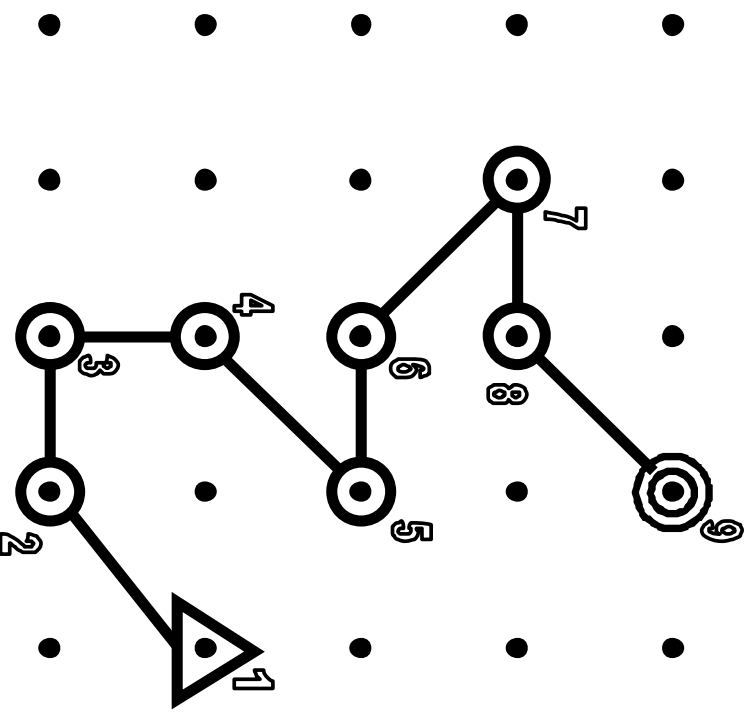
Circuit

8

B



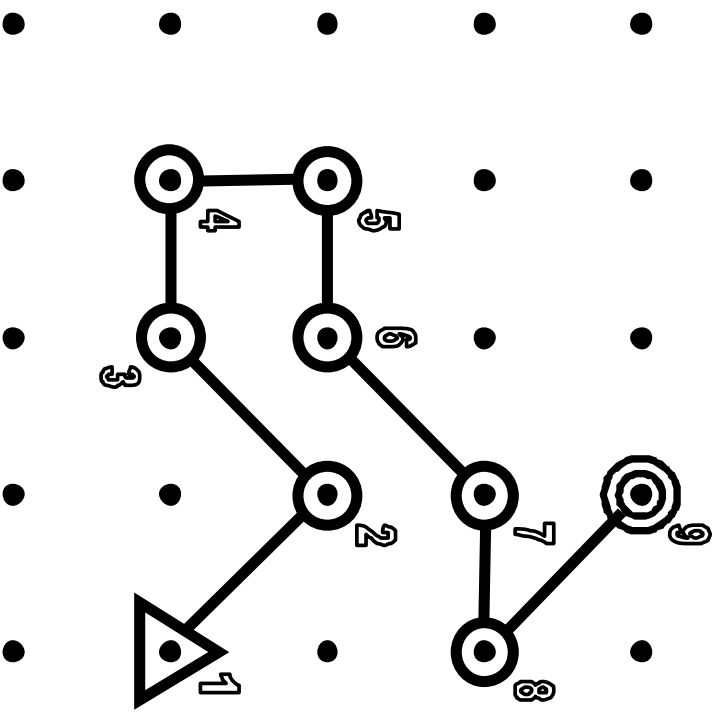
Δ
Départ

[illegible]

Nom :



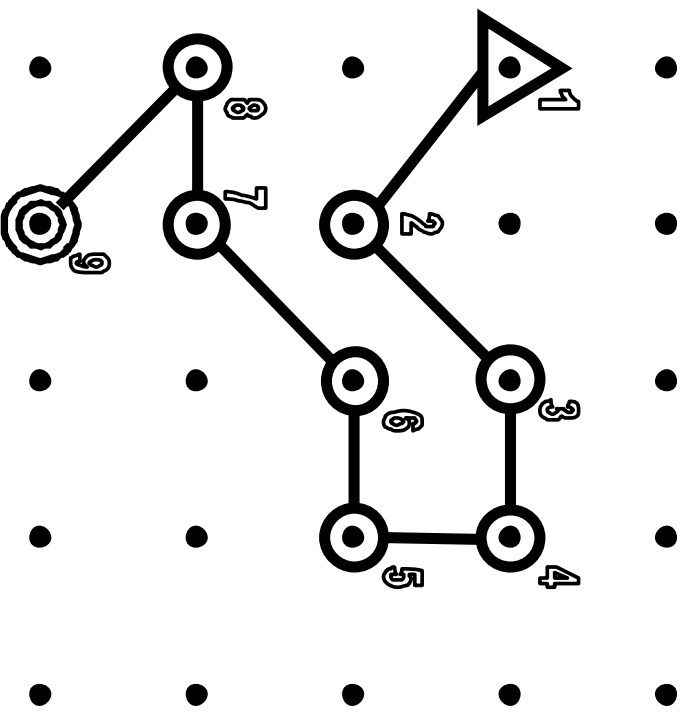
 Arrivée



Nom :



Arrivée



1	2	3	4	5	6	7	8	9	10	11	12
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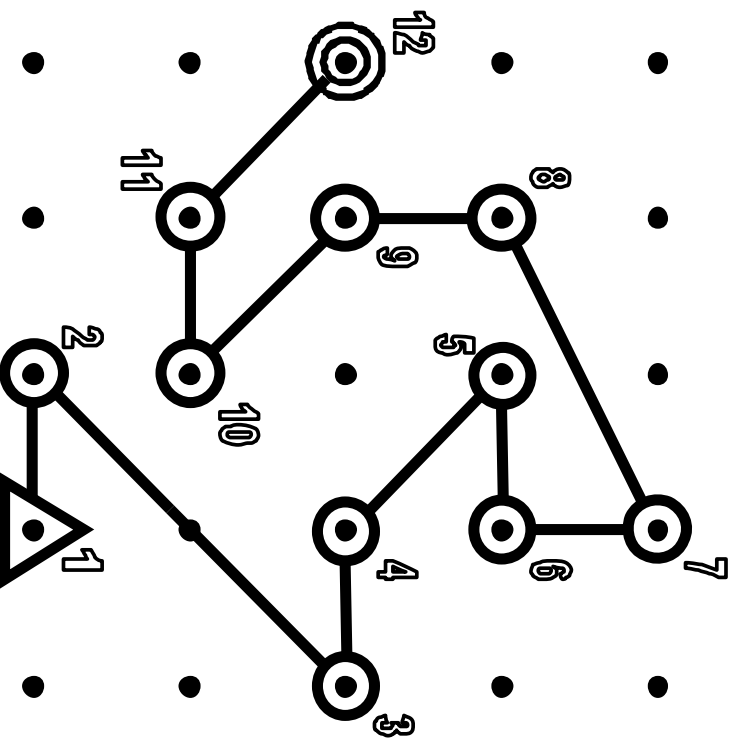
A

Nom :

Circuit
10
A



Arrivée

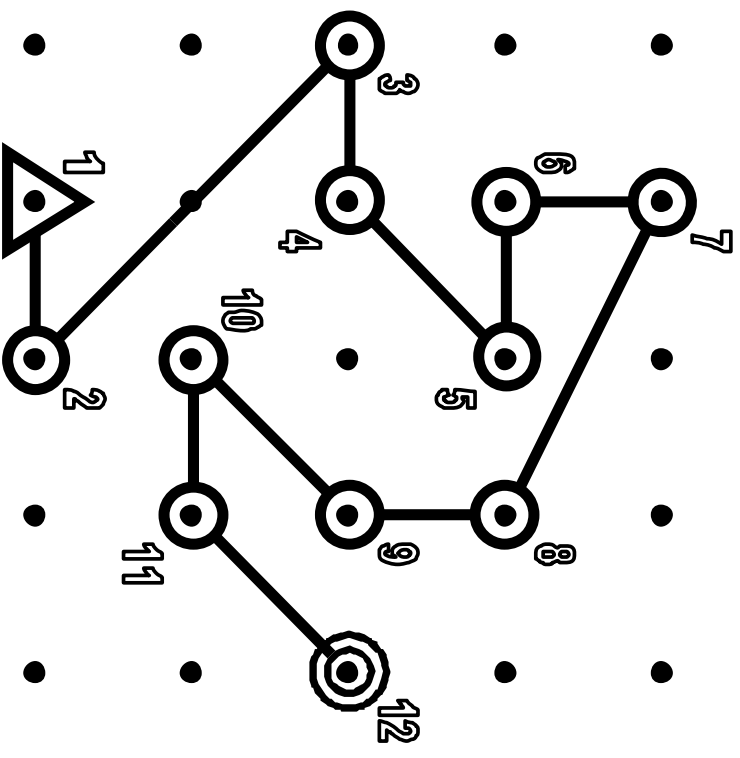
[illegible]

Nom :

Circuit
10
B



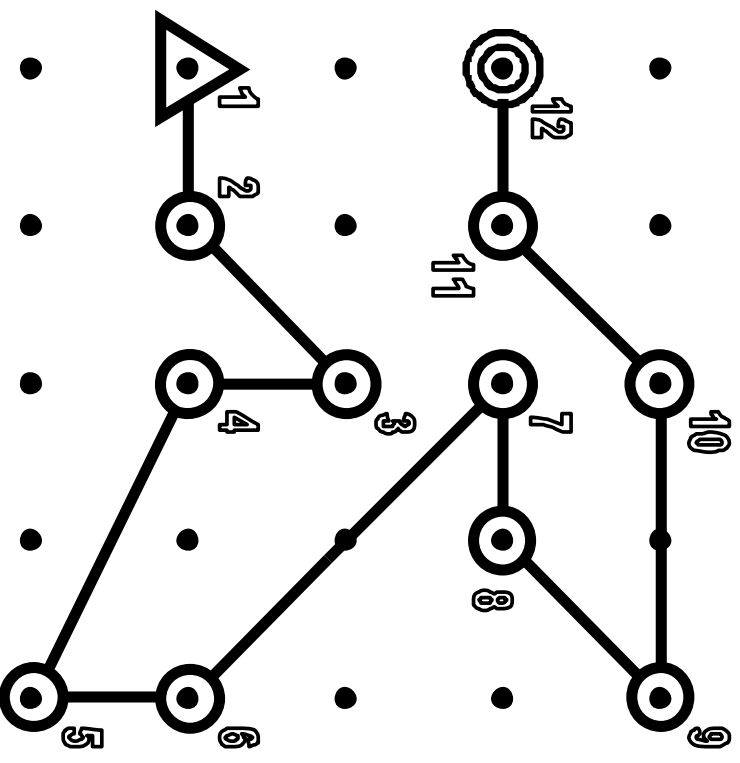
 Arrivéa

[illegible]

Nom :



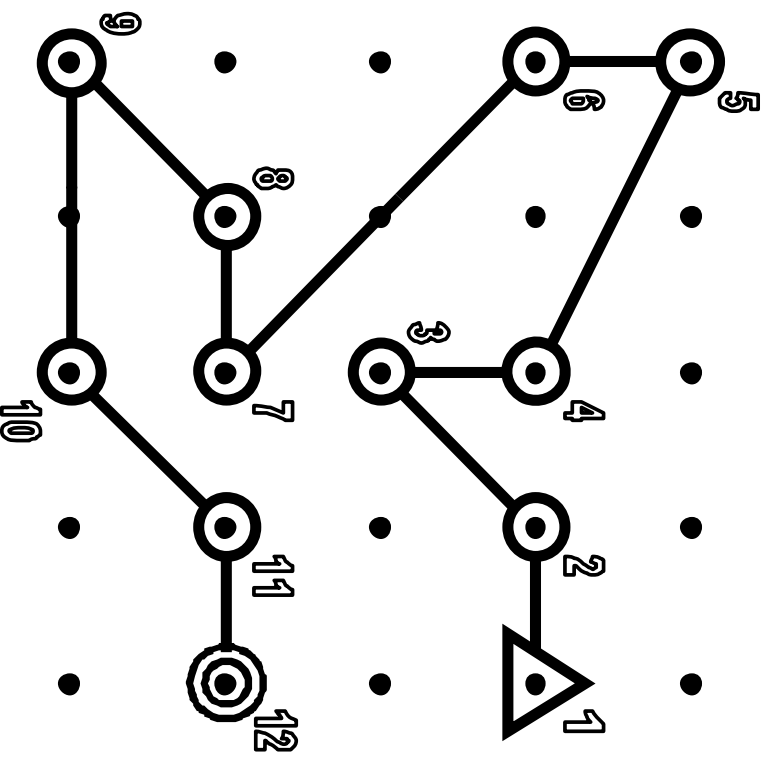
Arrivée

[illegible]

Nom :

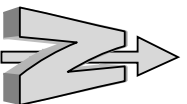
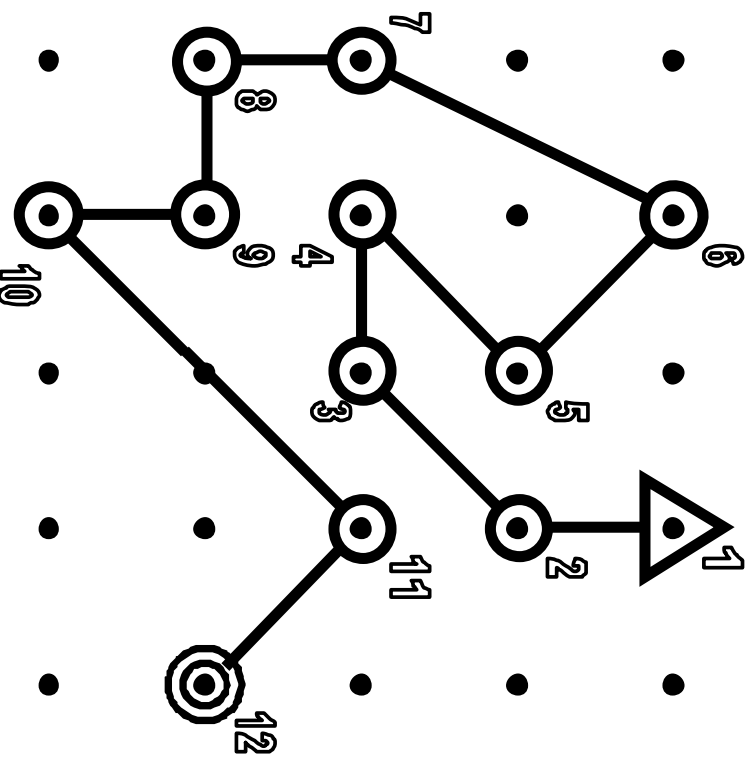


O Arrivée

[illegible]

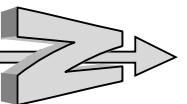
Nom :

Circuit
12
A

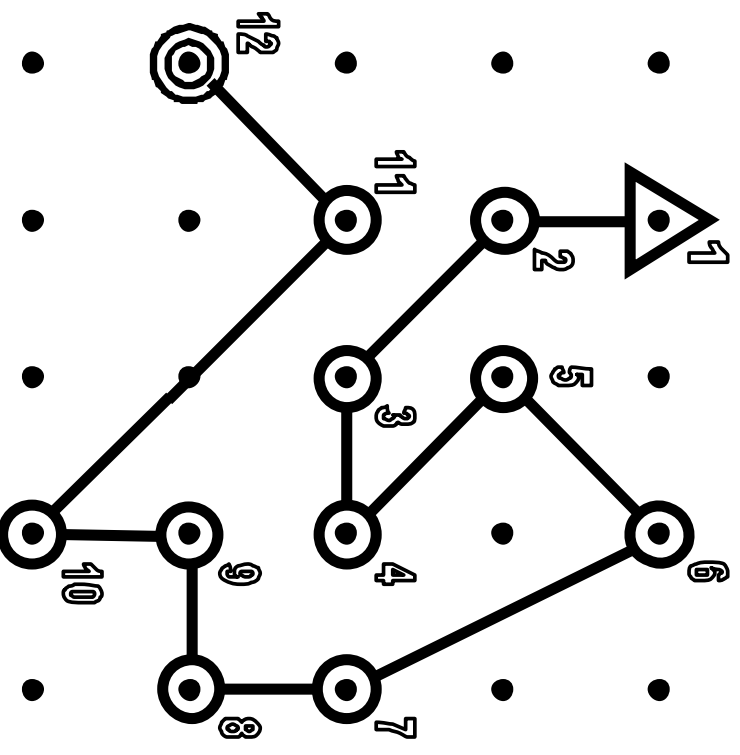
Départ [illegible]

Nom :

Circuit
12
B



Δ
Départ

[illegible]